

Further, it was alleged on page 6 of the Office Action of 10/26/2007 that "the apertures 504 are offset from the chips [30, 31]."

Referring to paragraph 0050 of Ku, the thermal bridge 50 includes at least one aperture 504, which is used "to accommodate the chips for saving material and facilitating the flow path design in forming the encapsulant 20 on the substrate 10."

However, there is no teaching or suggestion in Ku that the at least one aperture 504 of the thermal bridge 50, which is embedded by encapsulant 20, can somehow be adjusted in size to "effectively release the thermal stresses from the heat sink" *as claimed*, regardless of whether the aperture 504 is offset from the chips 30 and 31.

Moreover, since the aperture 504 of the thermal bridge 50 in Ku is embedded by the encapsulant 20, the thermal bridge 50 with aperture 504 is not capable of releasing thermal stresses, as required in independent claim 1.

In contrast, according to the Applicant's claimed invention, at least one hollow part extends through a heat sink, and "is formed at an area of the heat sink free of contact with the first chip and the semiconductor package" (independent claim 1). For example, as shown in FIGS. 4a-4b of the application, a heat sink 34 is formed with hollow parts 34a positioned at an area of the heat sink 34 free of contact with a first chip 32 and semiconductor packages 33. Therefore, thermal stresses can be effectively released through the at least one hollow part.

The Ku reference also does not teach or suggest a multi-chip package device in which **at least one semiconductor package** is mounted on and electrically connected to a surface of the chip carrier, where the heat sink is mounted on a surface of a chip and a surface of the semiconductor package.

On page 3 of the Office Action of 10/26/2007, the encapsulant 20 of Ku was cited as allegedly corresponding to the Applicant's claimed "at least one semiconductor package."

However, in Ku, the encapsulant 20 is used to encapsulate and seal the chips 30, 31 on a substrate 10, and the thermal bridge 50 (see, e.g., paragraph 0048 of Ku). Therefore, the encapsulant 20 does not correspond to the Applicant's claimed "at least one semiconductor package." One of ordinary skill in the art would know that an encapsulant and a semiconductor package do not have the same structure and/or function in the field of semiconductor packaging. Moreover, one of ordinary skill in the art would not have sufficient teaching or motivation to substitute a semiconductor package for the encapsulant 20 disclosed in Ku.

Further, the Ku reference does not teach or suggest a multi-chip package device in which the semiconductor package is mounted on the surface of the chip carrier, and "the semiconductor package is slightly thicker than the first chip" *as claimed*.

Regarding the rejection of claim 6, as shown in FIG. 4 of Ku, the chips 30 and 31 clearly are not mounted at the center of the substrate 10.

For at least the reasons discussed above, the Ku reference does not anticipate or otherwise render obvious the Applicant's claimed invention. Therefore, independent claim 1 and dependent claims 2-8 are patentable over Ku.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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